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| UNIVERSITY OF INFORMATION TECHNOLOGY  **COMPUTER ENGINEERING DEPARTMENT** | **FINAL EXAMINATION II (2019-2020)**  **COURSE: DEGITAL LOGIC DESIGN**  *Time duration: 90 minutes*  *(Paper materials are not allowed)*  *(OEP Students do the test by English,*  *Regular Students do the test by Vietnamese)* |

# Question 1: (5 points)

1. What is combinational circuit? Describe 5 combinational circuits

* Combinational circuit is the circuit whose outputs only depend on the inputs and change as the inputs change.
* 5 combinational circuits: adder, decoder, mux, subtractor, demux, comparator,

1. What is sequential circuit? Describe 5 sequential circuits

* Sequential circuit is the circuit whose outputs depend on the both inputs and previous states.
* 5 sequential circuits: latch, flipflop, counter, memory, fifo, lifo, …

1. Describe 5 memory components

* 5 memory components: RAM, ROM, Flash, Cache, hard disk (HDD).

1. What is Register Transfer Logic (RTL) design?

* RTL design is the design in which the data is performed by functional units, then transferred to other registers in each state. Using RTL design model, we can save the number of usage registers by reuse, sharing, merging registers, we also can speed up design by applying the pipeline techniques.

1. How can we determine the operation frequency of a design circuit?

* First, we determine the critical path between two registers, then measure its path delay. This delay is considered as clock cycle, the operation frequency is 1/ clock cycle.

1. Compare the disadvantages and advantages between the single cycle design and the multiple cycle design?

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|  | Single cycle design | Multiple cycle design |
| Advantages | Simple design | Small cycle time  Can apply pipeline to speed up design |
| Disadvantages | Big cycle time  Cannot apply pipeline to speed up design | Complex design  Need more hardware resource |

1. What is the main purpose of a pipelined functional unit design?

* The main purpose of a pipelined functional unit design is to reduce the cycle time.

1. What is the main purpose of a pipelined datapath design?

* The main purpose of a pipelined datapath design is to reduce the number of cycles when processing multiple input pairs.

1. What is difference between register sharing technique and register merging technique?

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| Register sharing technique | Register merging technique |
| Data can be stored in the same register in different states | Registers can use the same input, output ports. |

1. What is difference between resource-constraint scheduling and time-constraint scheduling?

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| Resource-constraint scheduling | Time-constraint scheduling |
| managing and allocating limited resources to tasks | prioritizes meeting specific time requirements or deadlines for tasks |

# Question 2: (2 points)

1. Show a Moore-based Finite-state machine (4 states) with datapath (FSDM) architecture of a system design.



1. Show a Mealy-based Finite-state machine (7 states) with datapath (FSDM) architecture of a system design.

